REMARKS

Claims 1-18 are pending in this application. Claims 1-6 were variously rejected under 35 U.S.C. § 112, second paragraph. Claims 1-3, 7-9 and 13-15 were variously rejected under 35 U.S.C. § 103(a). Claims 10-12 and 16-18 were objected to. Drawing Figures 1 and 4 were variously objected to under 37 C.F.R. 1.84(p)(5).

The amendments herein are made solely to promote prosecution without prejudice or disclaimer of any previously claimed subject matter. With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter and moreover has not acquiesced to any rejections and/or objections made by the Patent Office. Applicant expressly reserves the right to pursue prosecution of any presently excluded subject matter or claim embodiments in one or more future continuation and/or divisional application(s).

Applicant has carefully considered the points raised in the Office Action and believes that the Examiner's concerns have been addressed as described herein, thereby placing this case into condition for allowance.

Drawings

Drawing Figures 1 and 4 were objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include certain reference signs mentioned in the description. Figure 1 was also objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because it includes certain reference signs not mentioned in the description. Drawing Figure 1 was additionally objected to for failure to designate a legend indicating only that which is old is illustrated. Applicant respectfully traverses these objections.

Regarding Figure 1, the Examiner stated that the following reference signs were mentioned in the description and not included in Figure 1: "'first column 210,' 'SPE 200,' 'POH data 210' (see page 2, lines 11-13; Figure 1)." *See* 19 February 2004 Office Action, page 2 (hereinafter "Office Action"). The Examiner also stated that the following reference signs were

included in Figure 1 and not mentioned in the description: "Figure 1, '110,' '112.'" *See id.* Finally, the Examiner requested that Figure 1 be designated by a legend such as "--Prior Art--." *See id.*

Regarding Figure 4, the Examiner stated that the following reference signs were mentioned in the description and not included in Figure 4: "'pipeline 402,' 'pipeline 404' (see page 1, lines 11, 19, 26, 28-29; Figure 4)." *See id.*

Accordingly, Applicant has amended the specification paragraph at page 2, lines 1-16 to as follows: (1) "first column 210" (page 2, line 11) has been amended to "first column 112," (2) "SPE 200" (page 2, line 12) has been amended to "SPE 110," and (3) "POH data 210" (page 2, line 13) has been amended to "POH data 112." Reference signs "210" and "200" in the first paragraph of page 2, as originally filed, constitute typographical errors, which should have been labeled "112" and "110," respectively. Figure 1 contains no reference signs labeled "210" and "200," but does indeed include reference signs labeled "112" and "110" that match the written specification at page 2, lines 1-16, as now amended. Applicant's specification amendment of the reference signs "210" and "200" to "112" and "110," respectively, also moots the Examiner's objection that the reference signs "110" and "112" in Figure 1 are not mentioned in the description.

Figure 1 has been corrected to include the legend "--Prior Art--" per the Examiner's request.

Figure 4 has been corrected to include the reference signs "402" and "404" per the Examiner's request. Corrected drawing Figure 4 includes the reference sign "402" near the text "Pipeline 1 (CH 0)" and the reference sign "404" near the text "Pipeline 2 (CH0)." These corrections are consistent with the written description language at page 11, lines 11, 19, 26, 28-29, referring to Figure 4.

Attached to this response are corrected drawings for Figures 1 and 4.

Applicant respectfully submits that no new matter has been added by the above amendment and corrections, and that the specification and Figures 1 and 4, as amended, are fully supported by the specification of the present application for patent.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the Examiner's objections to Figures 1 and 4 under 37 C.F.R. 1.84(p)(5).

Rejection under 35 U.S.C. § 112, second paragraph

Claims 1-6 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. Applicant respectfully traverses this rejection.

Although Applicant believes that the claims were sufficiently definite when considered in view of the specification and the understanding of those of skill in the art, Applicant has attempted to respond to the concerns of the Examiner in order to enhance clarity and to facilitate disposition of the present case.

Regarding claim 1, the Examiner noted that claim 1 recites a limitation of "said first plurality of bytes processed by a *neighboring byte processing engine* is designated as a delineation byte." Office Action, page 3. The Examiner stated that claim 1 "does not mention a neighboring engine." *Id.*

Applicant has amended the language of claim 1 to clarify that the "neighboring byte processing engine" is from the group of "said plurality of parallel byte processing engines" previously described in claim 1. Applicant respectfully submits that no new matter has been added by the above amendment and that claim 1, as amended, is fully supported by the specification of the present application for patent. Applicant also respectfully submits that, as amended, claim 1 is now definite and the Examiner's rejection under 35 U.S.C. § 112, second paragraph has been overcome.

Regarding claims 2-6, the Examiner rejected the claims as being dependent on rejected claim 1. In light of Applicant's amendment and clarification to claim 1 and because claims 2-6 are dependent upon claim 1, Applicant respectfully submits that the Examiner's rejections of claims 2-6 under 35 U.S.C. § 112, second paragraph have been overcome.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the Examiner's rejections of claims 1-6 under 35 U.S.C. § 112, second paragraph.

Rejection under 35 U.S.C. § 103(a)

Claims 1-3, 7-9, and 13-15 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Hadziomerovic (EP 0147086) ("Hadziomerovic") in view of Bagheri et al., "10 Gb/s Framer/Demultiplexer IC for SONET STS-192 Applications," 1995 IEEE ("Bagheri"). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner stated that Hadziomerovic teaches an apparatus for processing data stream bytes, receiving data from a data channel during clock cycles, and generating data regarding the status of bytes. The Examiner also stated that Hadziomerovic "teaches the indication of a flag byte" and the cited art "discloses using flags for designating delineating bytes." Office Action, page 4. The Examiner stated that Hadziomerovic "teaches serial, instead of parallel processing" and the cited art "does not explicitly teach an 'input formatter' as disclosed in the claims." *Id.* The Examiner stated that Bagheri "teaches a data stream, where serial data is converted into 'a byte parallel, frame-synchronized output data stream.'" *Id.* The Examiner further stated that "[o]ne of ordinary skill in the [art] would have been motivated to apply parallel communication, as disclosed by Bagheri et al., since the disclosure teaches bandwidth optimization ... in a SONET (Synchronous Optical Network) environment." *Id.* Applicant respectfully disagrees with the Examiner's characterization of Hadziomerovic and Bagheri and submits that claim 1 is not unpatentable over Hadziomerovic in view of Bagheri.

Neither Hadziomerovic nor Bagheri teach or suggest an apparatus for the parallel processing of bytes from a data channel (e.g., HDLC, ATM, etc.). Hadziomerovic is directed to the problem of transmitting multiple channels of data over only one communication path. Hadziomerovic, page 1, lines 13-15 ("With increasing data communications, a need exists to facilitate transmission of multiple DLC channels over a single communications path"). Hadziomerovic teaches an apparatus for the multiplexing and demultiplexing of data link control ("DLC") channels (like HDLC). *See id.*, page 2, lines 1-22. The Hadziomerovic apparatus can combine multiple DLC channels of data into one data stream (*see, e.g., id.*, claim 1, page 23, lines 1-29) and extract multiple DLC channels from a single data stream (*see, e.g., id.*, claim 13, page 23, lines 8-34). Hadziomerovic further teaches the use of flag bytes to delineate the status of bytes and location of "bit oriented protocol frames" / DLC channels. *See id.*, page 2, lines 1-22; page 2, lines 23-35 and page 3, lines 1-8.

As is well known in the art, when a SONET frame is received by a byte processing apparatus, the delineation of the frame into bit oriented protocols / DLC channels (e.g., HDLC, ATM, etc.) and, ultimately, valid user data typically involves two separate stages of byte processing to determine the presence of flag bytes and delineation characteristics: (1) the SONET frame is processed to identify and extract data channel bytes, and then (2) each set of data channel bytes are processed to locate and set the status of valid user data bytes. As further discussed *infra*, however, Hadziomerovic only teaches the first stage, extraction of data *channels* from a communication path (e.g., SONET), and not the second stage of processing of the *bytes* in those data channels (e.g., HDLC, ATM, etc.) as claimed in the present invention.

Even assuming *arguendo* that the extraction of data channels from a single communication path is analogous to the processing of bytes from those data channels, Hadziomerovic still would not render the present invention obvious. As recognized by the Examiner, Hadziomerovic only teaches the processing (multiplexing and demultiplexing) of bytes

from a data stream in serial, and not in parallel as in claim 1 of the present application. Because the apparatus taught in Hadziomerovic operates in serial, flag bytes are processed sequentially (before or after a delineating byte). Thus, the determination of a delineation byte is a straightforward task: a flag byte will delineate a byte that immediately precedes or follows the flag byte. The efficient determination of a delineating byte through *parallel processing* in the present invention is more challenging. As demonstrated above, the status of any given byte from a data stream depends on the status of another byte. Thus, if bytes are processed in parallel without any communication between the processing engines, the bytes cannot be properly delineated because there is no information available in the same clock cycle regarding the other parallel processed bytes (or, in one embodiment, information regarding bytes in the previous clock cycle). If communication between the processing engines regarding byte status requires additional time or processing clock cycles, the bandwidth gains of processing in parallel are diminished. Thus, a novel aspect of the present invention lies in the processing of data stream bytes in parallel and communicating byte status information to other byte processing engines during the same processing cycle. Accordingly, claim 1 of the present invention is not rendered obvious by the teachings in Hadziomerovic.

Moreover, Hadziomerovic in view of Bagheri does not teach or suggest efficient parallel processing of data stream bytes. Bagheri teaches the conversion of a "serial bit stream into a byte-parallel, frame synchronized output data stream." Bagheri, p. 428. Bagheri also teaches an apparatus that "integrate[s] the framing and demultiplexing functions on a single chip ...." *Id.* The Bagheri apparatus loads a single byte from a SONET frame in parallel (two 4-bit segments) into two 4-bit shift registers, checks the byte with a "byte aligner," and loads a valid byte in parallel into two 4-bit latches. The byte is then examined to determine the SONET framing pattern. The byte output of the two latches are then "sent off-chip using output buffers ... for parallel signal processing." *Id.* Thus, Bagheri can take a raw serial bit stream of SONET data and efficiently demultiplex the stream into byte-parallel output of multiple data channels (e.g., HDLC, ATM, etc.). However, like

Hadziomerovic, Bagheri does not discuss or anticipate how those parallel outputted data channels will be further processed. And like Hadziomerovic, Bagheri does not address the problem of how to communicate information regarding other bytes while still processing bytes in parallel.

The present invention is completely distinguishable by teaching further processing of data channel bytes in parallel from a data channel that has been *already received* from a demultiplexer (such as a Bagheri or Hadziomerovic apparatus). Notably, claim 1 of the present invention describes an apparatus wherein the parallel byte processing engines in claim 1 "*receiv[e]* a first plurality of bytes from a *data channel*." (emphasis added); *see also, e.g.,* Detailed Description of the Invention, page 4, lines 27-30 ("Referring to Figure 2, a PTU 200, in accordance with one embodiment of the present invention, includes a *receiver channelizer unit* 202 for *demultiplexing* a SONET data stream into respective channels contained within the data stream.") (emphasis added). A Hadziomerovic or Bagheri demultiplexer may be *part* of an embodiment of the present invention and used to separate a SONET frame into different data channels for further processing, but neither reference teaches the subsequent processing of data stream bytes in parallel and communicating byte status information to neighboring byte processing engines in parallel.

Regarding motivation to combine references, the Examiner stated that "[o]ne of ordinary skill in the [art] would have been motivated to apply parallel communication, as disclosed by Bagheri et al., since the disclosure teaches bandwidth optimization ... in a SONET (Synchronous Optical Network) environment." Office Action, page 4 (emphasis added). However, as discussed *supra*, Applicant respectfully submits that Bagheri does *not* disclose "parallel communication" in its teachings. Rather, Bagheri only teaches extraction of data channels into parallel *output*. Bagheri, p. 428. The mere fact that Bagheri teaches bandwidth optimization in the Introduction section, without any further discussion of processing bytes in parallel, would not suggest to one of ordinary skill to apply communication between parallel byte processing engines, as recited in claim 1. Thus, it would not be obvious that because Bagheri generally teaches bandwidth optimization and

specifically teaches extraction of data channels into parallel *output*, the bytes of each of those output data channels should or could be further *processed* in parallel using parallel communication. Therefore, Applicant respectfully submits that claim 1 is patentable over Hadziomerovic in view of Bagheri.

Because claim 2 and 3 are dependent upon claim 1, Applicant respectfully submits that claims 2 and 3 are also patentable over Hadziomerovic in view of Bagheri, for the reasons discussed above.

Regarding claim 7, the Examiner again stated that Hadziomerovic teaches an apparatus for processing data stream bytes, receiving data from a data channel during clock cycles, generating data regarding the status of bytes, and using flags to delineate bytes. Office Action, page 5. The Examiner also stated that Hadziomerovic does not teach parallel processing or an "input formatter means" as recited in claim 7. The Examiner further stated that one of ordinary skill in the art would have been motivated to "apply parallel communication, as disclosed by Bagheri et al.," rendering claim 7 of the present invention obvious. Applicant respectfully disagrees with the Examiner's characterization of Hadziomerovic and Bagheri and submits that claim 7 is not rendered obvious by Hadziomerovic in view of Bagheri.

As discussed above, Hadziomerovic and Bagheri do not teach an apparatus for the parallel processing of bytes from a data channel and other claimed aspects of the present invention. The claimed apparatus in claim 7 of the present invention is patentable over Hadziomerovic and Bagheri as described in detail previously and as follows: First, both Hadziomerovic and Bagheri only teach the extraction and insertion of multiple data *channels* in a single communication path (e.g., multiplexing and demultiplexing SONET frames), and not the processing of the *bytes* in those data channels (HDLC, ATM, etc.) as claimed in claim 7.

Second, even assuming *arguendo* that the extraction of data channels is analogous to the processing of bytes from those data channels, Hadziomerovic in view of Bagheri still would not

render claim 7 obvious. As discussed above, because the status of any given byte from a data stream depends on the status of another byte, the serial processing of bytes is a straightforward task, while the efficient processing of bytes in parallel is a much more complicated endeavor. Neither Hadziomerovic nor Bagheri teach or suggest processing of data stream bytes in parallel and communicating byte status information to other parallel byte processing engines during the same processing cycle, the novel invention claimed in claim 7.

Third, Bagheri only teaches parallel *output* of data channels and not parallel *processing* of bytes from data channels, as recited in claim 7. Hadziomerovic only teaches serial processing of bytes. Thus, it would not be obvious to one of ordinary skill in the art that because Bagheri generally teaches bandwidth optimization and specifically teaches extraction of data channels into parallel *output*, the bytes of each of those output data channels should or could be further *processed* in parallel.

Therefore, in view of Applicant's previous remarks for claim 1 and the responses set forth above for claim 7, Applicant respectfully submits that claim 7 of the present invention is patentable over Hadziomerovic in view of Bagheri.

Because claim 8 and 9 are dependent upon claim 7, Applicant respectfully submits that claims 8 and 9 are also patentable over Hadziomerovic in view of Bagheri, for the reasons discussed above.

Regarding claims 13-15, the Examiner stated that because the "claimed method includes the steps of 'receiving', 'generating', and 'processing,'" that the "combination of prior art cited in the present Office action teaches or suggests limitations corresponding to the apparatus (see Rejections above) and therefore, the method." Office Action, page 6. Consequently, the Examiner rejected claims 13-15.

As discussed above, Applicant refers to his responses for claims 1-3 and 7-9 demonstrating the various reasons why Hadziomerovic in view of Bagheri does not teach nor

suggest, together or separately, the present invention. Because the Examiner rejected claims 13-15 only with reference to the "combination of prior art cited in the present Office action," Applicant respectfully submits that claims 13-15 of the present invention are patentable over Hadziomerovic in view of Bagheri.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-3, 7-9, and 13-15 under 35 U.S.C. § 103(a) for unpatentability over Hadziomerovic in view of Bagheri.

Dependent Claim Objections

Claims 10-12 and 16-18 were objected to as being dependent upon a rejected base claim.

Applicant respectfully submits that all of the Examiner's rejections to base claims 7, 10, 13, and 16 have now been overcome as set forth above, and respectfully requests reconsideration and withdrawal of the Examiner's objection to claims 10-12 and 16-18.

Additional Prior Art

Regarding the three additional prior art references stated by the Examiner on page 7 of the Office Action, Applicant notes that none of these references teach parallel byte processing and parallel communication as recited in claims 1, 7, and 13 of the present invention and therefore respectfully submits that all claims of the present invention are not obvious in view of Robe et al., "A SONET STS-3c User Network Interface Integrated Circuit," Begur et al. (US 5,784,649) and/or Bernardini (US 5,144,623).

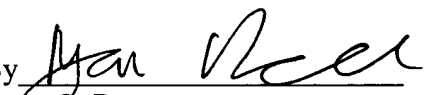
CONCLUSION

Applicant respectfully submits that all issues raised in the Office Action have been properly addressed in this response, and that all pending claims 1-18 are now in condition for allowance. Accordingly, reconsideration and allowance of the pending claims is respectfully requested. If the Examiner feels that a telephone interview would serve to facilitate resolution of any outstanding issues, the Examiner is encouraged to contact Applicant's representative at the telephone number below.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorize the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 388682000700.

Dated: June 21, 2004

Respectfully submitted,

By 

Ryan G. Roemer
Registration No.: 55,872
MORRISON & FOERSTER LLP
3811 Valley Centre Drive, Suite 500
San Diego, California 92130
(858)-314-5417

Replacement Sheet

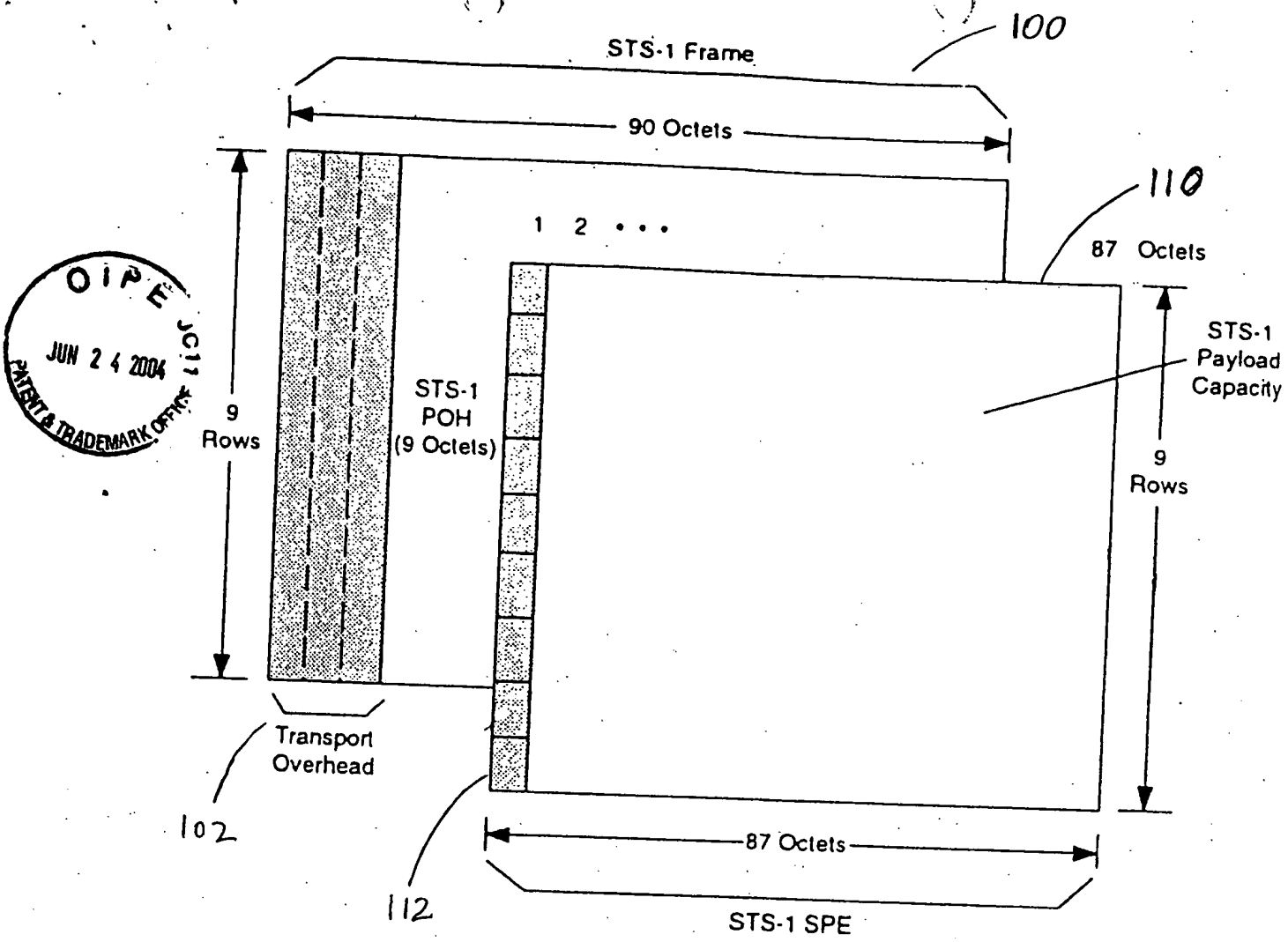


Figure 1

--Prior Art--

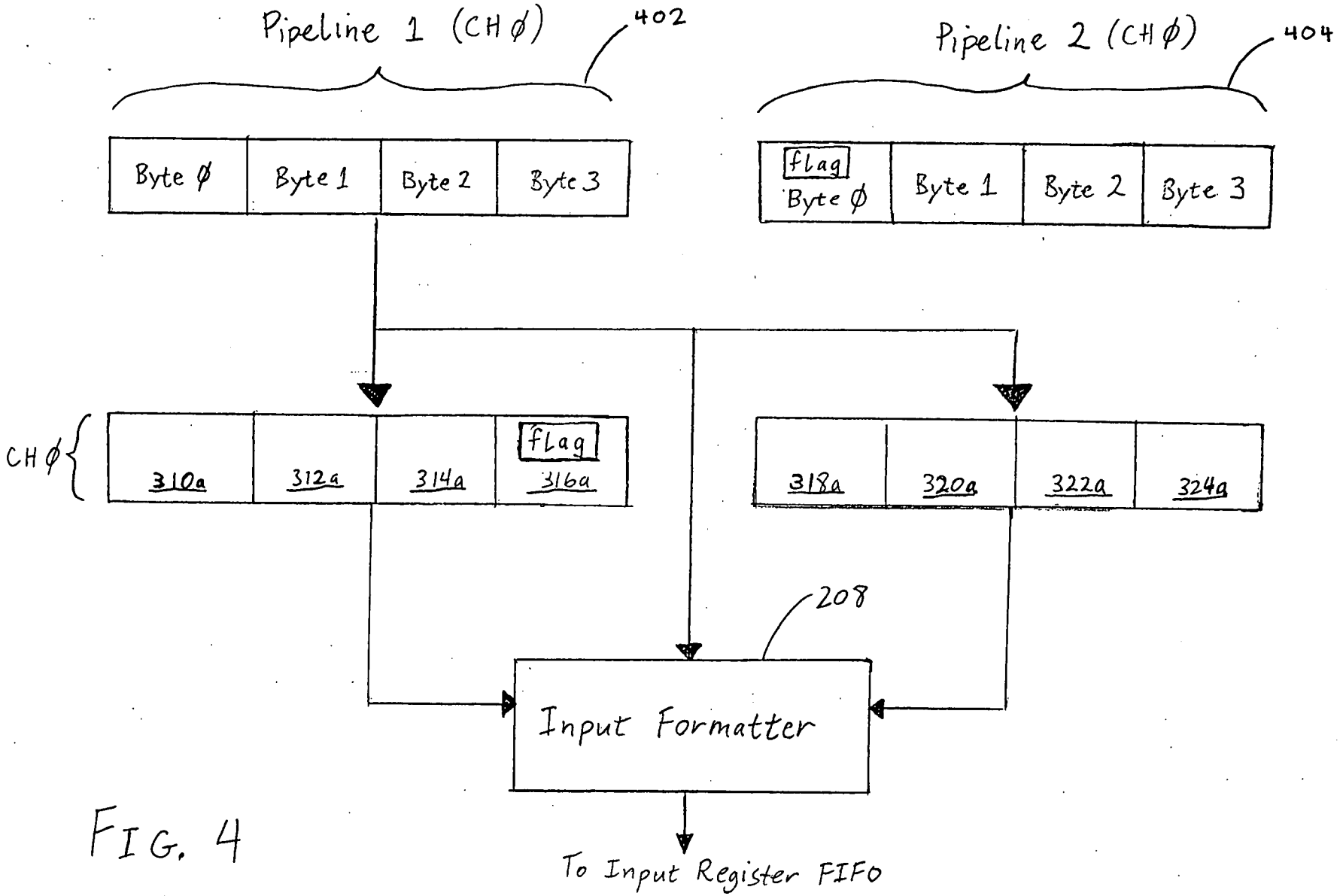


FIG. 4